CENG 450

Post-lab Summary

January 28th, 2014

Lab Session 1

Lab session 1 comprised of the introduction to the Xilinx program and a tutorial on how to create, modify, test and implement elements of a Xilinx project. The tutorial guided us through the creation of a Xilinx project and using pre-existing VHDL module that simulated memory. The modules consisted of the ROM, which defined the data in memory, the counter, which defined the memory address, and a module that controlled them both.

First, a testbench was created to analyze the program at certain inputs. We expected that once the EN switch was closed, the counter would display the data at the next address. Additionally, if the resent button was pushed, the counter would reset. This is in fact what occurred in the simulation.

Next, the program was transferred to the FPGA, using the pins we had defined. We expected to see the same results as in the simulation, with the output being represented by LEDs. After programming the chip, and flipping the switch, values began to appear on the LED’s according to the clock cycle. Pressing the reset button started the sequence over.

In Part two, we recreated the above setup graphically, by importing the third module as a chip. We were then able to assign inputs to the chip and define outputs. Once this had been completed, a testbench was created as before, with the same results. Finally, the program was again transferred to the FPGA, and verified.